



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/402,021	09/27/1999	MINORU TSUJI	KOIK-P9143	5446

26263 7590 02/23/2007
SONNENSCHN NATH & ROSENTHAL LLP
P.O. BOX 061080
WACKER DRIVE STATION, SEARS TOWER
CHICAGO, IL 60606-1080

EXAMINER

SELLERS, DANIEL R

ART UNIT	PAPER NUMBER
----------	--------------

2615

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/23/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

09/402,021

Applicant(s)

TSUJI ET AL.

Examiner

Daniel R. Sellers

Art Unit

2615

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04 December 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-3,5-7,9-15,18,19 and 25 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3,5-7,9-15,18,19 and 25 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 27 September 1999 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. **Claims 1-3, 5-7, 9-15, 18, 19, and 25** are rejected under 35 U.S.C. 103(a) as being unpatentable over Shishido et al., USPN 5,869,782 and Ware et al., USPN 5,537,573 (hereinafter Shishido and Ware).

3. Regarding **claim 1**, Shishido teaches a method comprising the steps of:
storing a data block to be used repeatedly at least twice out of a plurality of data blocks obtained at least by dividing a digital signal on a time base, said block being stored separately from said remaining data blocks (col. 2, lines 4-18 and col. 25, lines 27-32). Shishido discloses a method of MIDI file compression, wherein a block obtained by dividing a signal on a time base to be used repeatedly within a file is stored only once in the compressed file along with information to retrieve the original file. The repeated block is inherently stored separately from the other remaining data blocks, and the individual blocks in said remaining blocks are stored individually, or separately, from each other (i.e. a computer, as taught by Shishido, inherently can read or write blocks of memory individually because they are separatable by address). However, Shishido does not teach the steps of (1) receiving information indicating the period of time during which said data block is retained, wherein the period of time is related to each use of said data block and (2) deleting said data block based on said information.

Ware teaches a cache system for reducing latency and improving cache hit rate, or the likelihood that needed data is stored in a faster cache memory. Ware teaches the feature of receiving information indicating the period of time during which said data block is retained, wherein the period of time is related to each use of said data block, and deleting said block based on said information (col. 6, line 62 – col. 7, line 8). Ware teaches that a number of accesses, or uses, can indicate the period of time a block is retained. It would have been obvious for one of ordinary skill in the art to combine the teachings of Shishido and Ware for the purpose of providing a high cache hit rate and low latency (Ware, col. 2, lines 52-54). A high cache hit rate, in this context, would reduce the need for retrieving the reused data block over and over again from a slower solid-state memory or an even slower spinning drive.

4. Regarding **claim 2**, the further limitation of claim 1, Shishido discloses that a MIDI musical performance file may be taken into a recording medium by way of a network before it is reproduced (col. 2, lines 34-38 and lines 45-49).
5. Regarding **claim 3**, the further limitation of claim 1, Shishido discloses a digital signal recorded in a recording medium (col. 1, lines 49-51).
6. Regarding **claim 5**, the further limitation of claim 1, Shishido discloses a file that has timing information indicating periods of time to use data blocks and a system using flags to determine how the file is reproduced from memory (col. 9, lines 19-21, 47-48, and 55-57, col. 10, lines 11-22, and fig. 11). Ware teaches that a period of time starts when the data is read in, or accessed (col. 6, line 66 – col. 7, line 1).

7. Regarding **claim 6**, the further limitation of claim 1, see the preceding argument with respect to claim 1. Ware teaches that a predetermined period of time or a predetermined number of accesses determines when a block of data is removed from the cache

8. Regarding **claim 7**, the further limitation of claim 1, see the preceding argument with respect to claim 5. Ware teaches the use of a predetermined period of time to determine the time of deletion, and it is inherent that a predetermined time can be referenced from the start of processing.

9. Regarding **claim 9**, the further limitation of claim 1, see the preceding argument with respect to claims 5 and 7. Shishido, further, teaches the use of timing events, which inherently can be used to indicate the start of the period of time for retention.

10. Regarding **claim 10**, the further limitation of claim 1, see the previous office action. Shishido teaches the use of added information to compress the file. Ware teaches the use of timing information for retention and deletion purposes. It is obvious to combine the two as stated previously.

11. Regarding **claim 11**, the further limitation of claim 1, see the preceding argument with respect to claim 1. Ware teaches the use of timing information for retention and deletion purposes, wherein Ware is proposing a solution to cache misses and improving cache hits. Ware is also attempting to use the cache more efficiently (col. 5, lines 20-24). It is inherent to delete the block of data after it is used for a final time for these reasons.

Art Unit: 2615

12. Regarding **claim 12**, the further limitation of claim 1, see the preceding argument with respect to claim 11. It is inherent that to improve cache hits, the block would be retained until it was unnecessary.

13. Regarding **claim 13**, the further limitation of claim 1, see the preceding argument with respect to claim 11. It is inherent to delete the information when it becomes unnecessary for the purpose of efficient memory usage.

14. Regarding **claim 14**, the further limitation of claim 1, see the preceding argument with respect to claim 1. In this context, it is inherent that a predetermined bit string, in either hardware or software, defines a predetermined time period.

15. Regarding **claim 15**, Shishido teaches an apparatus comprising:

a first decoding means for separating a data block to be used repeatedly at least twice from the remaining data blocks of a plurality of data blocks obtained at least by dividing a digital signal on a time basis and decoding said data block, wherein said first decoding means extracts information indicating the period of time during which said data block is retained, wherein the period of time is related to each use of said data block; (Refer to claim 1. Furthermore, see Shishido, col. 4, lines 11-19. A first decoding means is disclosed.)

a retaining means for temporarily retaining said data block to be used repeatedly at least twice from said first decoding means separately from said remaining blocks (See Shishido, col. 9, lines 41-51 and lines 55-57. Shishido discloses a temporary retaining means for storing all the data blocks, which are inherently separable);

Art Unit: 2615

a second decoding means for decoding said remaining data blocks from said first decoding means and said data block to be used repeatedly at least twice from said retaining means (See Shishido, col. 4, lines 11-19. Shishido discloses a second decoding means for decoding remaining data blocks); and

control means for deleting said data block from said retaining means based on said information (It is inherent that the method Shishido discloses includes control means for memory management, and deleting, overwriting, or reallocation are basic functions of a memory management system).

Shishido teaches these features except for the information indicating a period of time for retention. As stated previously, Ware teaches the use of timing information for the purpose of retention.

16. Regarding **claim 18**, the further limitation of claim 15, Shishido discloses a second decoding means, where it uses information to identify the coded blocks by type (col. 4, lines 11-19 and col. 26, lines 25-34)

17. Regarding **claim 19**, the further limitation of claim 15, see the preceding argument with respect to claim 1 and 18. Shishido discloses a decoding means, wherein reproduction time information is used (col. 24, line 60 - col. 25, line 14).

18. Regarding **claim 25**, see the preceding argument with respect to claim 15. The combination of Shishido and Ware teach these features.

Response to Arguments

19. Applicant's arguments filed December 4, 2006 have been fully considered but they are not persuasive. As acknowledged by the applicant, Shishido teaches a method for MIDI file compression. The file compression can be considered a method of dividing a MIDI file, a file comprised of musical notes, on a time basis, wherein the file comprises repeated blocks of musical notes. Shishido relies on a decoder to decode the compressed file and "a musical data storage medium (13) for storing the decoded musical data temporarily" (col. 9, lines 47-48). The storage medium (13) inherently has a limited size for temporary storage, wherein blocks of data are inherently written and deleted. Shishido does not teach a time period indication for deleting the data from the temporary storage, however Ware teaches this missing feature. Ware teaches a cache that relies access times to determine what is removed from the cache, or the temporary storage medium (col. 6, line 62 – col. 7, line 8).

Ware teaches receiving information indicating the period of time during which the data block is retained, where the period of time is related to each use of the data block (col. 7, lines 2-5). Ware teaches that a block is retained until a predetermined number of accesses, or uses, has been reached.

The claims do not indicate specifically how the blocks are separate. In claim 1, the phrase "said data block being stored separately from said remaining data blocks" is given the broadest reasonable interpretation. Inherently the blocks must be separatable, which implies that they are stored separately (see corresponding rejection under 35 USC 103). Likewise, claims 15 and 25 are interpreted in a similar manner.

Art Unit: 2615

20. Regarding claims 1-3, 5-7, 9-15, 18, 19, and 25, see the current rejections under 35 USC 103.

Conclusion

21. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Rosenau et al., U.S. Patent 5,598,352, Gannon, U.S. Patent 5,990,407, and Abrams et al., U.S. Patent 6,658,309.

22. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel R. Sellers whose telephone number is 571-272-7528. The examiner can normally be reached on Monday to Friday, 9am to 5:30pm.

Art Unit: 2615

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sinh Tran can be reached on (571)272-7564. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DRS


SINH TRAN
SUPERVISORY PATENT EXAMINER